Amendments to drawing figures:

Please replace sheets 1 through 5 of the informal drawings with the attached replacement formal drawings.

REMARKS

The examiner has rejected claims 1, 2, 4-11, and 13-17 under 35 U.S.C. § 102(b) as being anticipated by Daniel et al, US Patent 5,848,068, hereinafter Daniel et al. This rejection is not thought to be well taken.

Both claims 1 and 10, the only independent claims in the application, specifically claim, in both method and structure form, limitations to a space in the buffer control block for links to other buffers *and* each buffer having a last bit flag bit that has a first position when an additional buffer is to be chained thereto, and a second position when no additional buffer is to be chained thereto. While Daniel et al have pointers to the next subsequent element (column 29, lines 48-50), the patent has nothing to compare to the space for the last bit flag bit, and the filing thereof. The examiner has cited column 30, lines 62-65, to show this; however, this location refers only to pointers, not to a last flag bit.

Prior art is anticipatory only if every element of the claimed invention is disclosed in a single item of prior art in the form literally defined in the claim. Jamesbury Corp. v. Litton Indus. Products, 756 F.2d 1556, 225 USPQ 253 (Fed. Cir. 1985); Atlas Powder Co. v. du Pont, 750 F.2d 1569, 224 USPQ 409 (Fed. Cir. 1984); American Hospital Supply v. Travenol Labs, 745 F.2d 1, 223 USPQ 577 (Fed. Cir. 1984).

Thus, clearly neither claim 1 nor claim 10 is anticipated by Daniel et al since Daniel et al do not show *both* pointers *and* last bit flag bits.

Claims 2, 4-9, 11 and 13-17 are dependent, directly or indirectly, on claims 1 or 10, and for the same reasons, are believed to be allowable. Moreover, claims 4 and 13 require error correction code, and claims 5 and 14 require parity bits. A reading of the locations cited by the examiner in the Daniel et al patent does not seem to reveal the presence of either error correction

code or parity bits, and in a review if the remainder of the Daniel et al patent, the undersigned attorney was not able to find a disclosure of either error correction code or parity bits. While error correction code and parity bits are not new *per se*, they are not taught by the single reference cited by the examiner. A possibility or probability that features of the prior art contained in the disclosure of the prior art is not enough to establish anticipation. The same characteristics must be a "natural result flowing" from what is disclosed (Continental Can Co. v. Monsanto Co., 20 USPQ2d 1746, 1749 (Fed Cir. 1991). Thus, for these additional reasons, claims 4, 5, 13 and 14 are believed to be allowable.

Claims 7 and 15 each contain a limitation to the buffer control block including the next buffer address when the last bit flag is in either position. Daniel et al could not show this for several reasons. First, Daniel et al have no last bit flag and, also, the last element of a list contains a "0" or "null value" (column 29, lines 50-52). Thus, for this additional reason, claims 7 and 15 are allowable.

The allowability of claims 3 and 12 is noted with appreciation. These claims have been rewritten as independent claims 18 and 19, respectively, and as such are believed to be allowable.

It is believed that all of the claims now in the application are distinguishable one from the other and over the prior art. Therefore, reconsideration and allowance of the claims are respectfully requested.

Respectfully submitted,

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